REMARKS

Status of Prosecution

Applicant filed the original application on April 5, 2001. The Examiner mailed a first, non-final Office Action on September 24, 2004. This paper is in Response to that Office Action. Applicant requests reconsideration and withdrawal of the rejections raised in that Office Action. Claims 1 through 20 are pending. In the instant Office Action, the Examiner rejected claims 1-20.

Claim Rejections

Rejections under 35 U.S.C. §102

The Examiner rejected claims 1-5 and 7-20 under 35 U.S.C. § 102(e) as anticipated by PCT Patent Application WO 01/05086 ("WO 0105086") to Krishna et al. The rejections are respectfully traversed.

For fundamental teaching on the doctrine of anticipation, one must consider the decision of Judge Rich in *In re William J. King*, 801 F.2d 1324, 231 U.S.P.Q. 136 (Fed. Cir. 1986):

> It is axiomatic that <u>anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim</u>, and that anticipation is a fact question subject to review under the clearly erroneous standard. *Lindemann Maschinenfabrik v. American Hoist and Derrick*, 730 F.2d 1452, 1457, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). Our review of a finding of anticipation is the same whether it was made by the board or by a district court.

In re William J. King, 801 F.2d at 1326 (emphasis added).

Further, for a reference to anticipate a claim under 35 U.S.C. §102, that reference must teach, or identically describe, each and every element or step of the claim. *See, e.g., Jamesbury Corp. v. Litton Industrial Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985). "Anticipation" is a restrictive concept, requiring the presence in a single prior art disclosure of each and every element of a claimed invention. The test for infringement by anticipation should be rephrased as, "That which would *literally* infringe if later in time anticipates if earlier than the date of the invention." *Lewman Marine, Inc. v. Barient, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766 (Fed. Cir. 1987) (emphasis in original). Further, as held in *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1896 (Fed. Cir. 1991), "there must be <u>no difference</u> between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention." (emphasis added). As

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discussed below, the WO 0105086 reference <u>does not disclose the identical structure</u> described in the Application.

<u>Claims 1-5</u>

Referring to independent claim 1, the Examiner cites to page 2, lines 3-11 and page 6, lines 22-26 of WO 0105086 as anticipating the element: "a first processor operating a software application having a multi-layer protocol." The text at page 2, lines 3-11 of WO 0105086 is contained in the "background of the invention" section of WO 0105086 and states:

> Recently, an industry security standard has been proposed that combines both "DES/3DES" encryption with "MD5/SHA1" authentication, and is known as "IPSec." By incorporating both encryption and authentication functionality in a single accelerator chip, over-all system performance can be enhanced. But due to the limitations noted above, the prior art solutions do not provide adequate performance at a reasonable cost.
>
> Thus it would be desirable to have a cryptography accelerator chip architecture that is capable of implementing the IPSec specification (or any other cryptography standard), at much faster rates than are achievable with current chip designs.

WO 0105086, page 2, lines 3-11. This text discusses the *desire* for a "cryptography accelerator chip architecture that is capable of *implementing the IPSec specification* (or any other cryptography standard), at much faster rates than are achievable with current chip designs." *Id.* at lines 9-11 (emphasis added). Such background information certainly does not anticipate or describe "a first processor operating a software application having a multi-layer protocol." There is no structure described.

The text at page 6, lines 22-26 of WO 0105086 only refers to a "processing unit" 114 of Fig. 1A, and a "local processing unit" 108 associated with a cryptography acceleration chip 102. It is unclear whether the Office Action points to processing unit 114 or the local processing unit 108 as anticipating the "first processor" element of claim 1. Either way, neither of the processors, 114 nor 108, are described as operating a software application having a multi-layer protocol, as discussed further below.

The text at page 3, lines 2-25 of the "summary of the invention" section of WO 0105086, cited as anticipating "a high performance processor configured to operate *one layer of the multi-layer protocol* according to a command from the first processor," simply states that the

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technology described in the WO 0105086 application "provides improved performance over the prior art designs." Id. at page 3, lines 10-11. The text also states:

> In one aspect, the present invention provides a cryptography acceleration chip. The chip includes a plurality of cryptography processing engines, and a packet distributor unit. The packet distributor unit is configured to receive data packets and matching classification information for the packets, and to input each of the packets to one of the cryptography processing engines. The combination of the distributor unit and cryptography engines is configured to provide for cryptographic processing of a plurality of the packets from a given packet flow in parallel while maintaining per flow packet order. In another embodiment, the distributor unit and cryptography engines are configured to provide for cryptographic processing of a plurality of the packets from a plurality of packet flows in parallel while maintaining pack ordering across the plurality of flows.

Id. at page 3, lines 15-25. There is no discussion of a processor configured to operate *one layer of a multi-layer protocol* according to a *command from a first processor.*

The "distributor unit" 206 (see Fig. 2 of WO 0105086) resides on the cryptography chip architecture 200 (Fig. 2) and "determines if a packet is ready for IPSec processing, and if so, distributes the security association information (SA) received from the packet classifier unit 204 and the packet data among a plurality of cryptography processing engines 124, in this case four, on the chip 200, for security processing." Id., page 8, lines 30-33. This distributor does not partition into subsequent hardware blocks, it distributes packets - without stripping the processing-intensive pieces - to the engines 124 in a round robin fashion. Id., page 9, lines 8-22. There is no discussion of a processor operating one layer of a multi-layer protocol according to a command from a first processor. Such per-flow ordering is instead a type of "horizontal" partitioning of processing. Further, the cryptography and authentication engines 214, which reside on the cryptography chip architecture 200 (Fig. 2 of WO 0105086), are not operating one layer of a multi-layer protocol according to a command from a first processor.

Note that in the configuration depicted in Fig. 1A, "packets are received from the LAN or WAN and *go directly through the cryptography acceleration chip* and are processed as they are received from or are about to be sent out on the WAN, providing *automatic security processing for IP packets*." Id., page 6, lines 31-34 (emphasis added). Again, there is no discussion of a

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processor configured to operate *one layer* of a multi-layer protocol according to a *command from a first processor*.

WO 0105086 distributes its processing in a horizontal fashion, distributing entire IP packets to identical processing blocks. There is no partitioning of one protocol layer out of multiple layers from one chip to another chip. The technology of WO 0105086 is more applicable to a custom application specific integrated circuit (ASIC) or custom hardware, and is not flexible or generically adaptable to partition one layer of a multi-layer protocol according to a command from a first processor to another processor.

For example, Fig. 3 of WO 0105086 demonstrates parallel processing of packets for high speed processing, but does not demonstrate partitioning of one protocol layer. See also, WO 0105086, page 5, lines 31-34, page 11, lines 16-35, and page 12, lines 1-4. Figs. 6A and 6B of WO 0105086 implies that all layers of processing are done in the same processing unit including header encapsulation and removal, encryption, decryption, and authentication. There is no indication of layered processing. See also, WO 0105086, page 18, lines 22-34 and page 19, lines 1-10.

The Office Action cites WO 0105086, page 7, lines 23-26 as anticipating "a memory accessible to each of the first processor and the high performance processor for passing commands and data between the first processor and the high performance processor." However, the "memory" referred to in this passage is a "local memory" 160 associated with the cryptography acceleration chip 152 configuration of Fig. 1B. WO 0105086, page 7, lines 23-24. Referring to Fig. 1B, it is clear that memory 160 is merely communicatively coupled to the cryptography acceleration chip 152 *only*. There is no indication of memory 160 being accessible to each of a first processor and a high performance processor for passing commands and data between the two and no discussion of such a function.

The Office Action also cites WO 0105086, page 8, lines 22-29 as anticipating the memory element of claim 1. This passage refers to a memory used by a classification engine for performing "lookups from databases" stored there. Id., page 8, lines 21-22. This memory is communicatively coupled to either a memory controller 212 or directly to the cryptography engines 216 [sic] and packet classifier 204. Id. at lines 22-26. There is no discussion or diagram indicating that this memory is accessible to each of a first processor and a high performance processor for passing commands and data between the two.

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None of the elements, alone or in combination, of independent claim 1 of the Application are disclosed in WO 0105086. The rejection of claim 1 is unsupported by the cited art and should be withdrawn. As WO 0105086 does not anticipate independent claim 1, WO 0105086 cannot anticipate dependent claims 2-5. The rejection of claims 2-5 is unsupported by the cited art and should be withdrawn.

Claims 7-11

Referring to independent claim 7, the Examiner cites to page 2, lines 3-11 of WO 0105086 as anticipating the element: "a multi-layer security protocol having one or more of an encryption algorithm and an authentication algorithm." As discussed above with respect to claim 1, the background information provided in these lines of text from WO 0105086 does not describe any anticipating structure.

The same lines of text are cited as anticipating the "shared memory" element of claim 7 as were cited as anticipating the "memory" element of claim 1. As discussed above with respect to claim 1, the "memory" referred to at page 7, lines 23-26 is a "local memory" 160 associated with the cryptography acceleration chip 152 configuration of Fig. 1B. WO 0105086, page 7, lines 23-24. Referring to Fig. 1B, it is clear that memory 160 is merely communicatively coupled to the cryptography acceleration chip 152 *only*. There is no indication of memory 160 being "shared".

The passage at page 8, lines 22-29 refers to a memory used by a classification engine for performing "lookups from databases" stored there. Id., page 8, lines 21-22. This memory is communicatively coupled to either a memory controller 212 or directly to the cryptography engines 216 [sic] and packet classifier 204. Id. at lines 22-26. There is no discussion or diagram indicating that this memory is shared between two processor elements, one of which operates "a first portion of a predetermined one of the security protocols, another of which operates "a second portion of the predetermined one of the security protocols."

Furthermore, WO 0105086 does not describe either of these two processor elements. As discussed above with respect to claim 1, WO 0105086 only partitions processing in horizontal fashion. WO 0105086 does not describe separating out first and second portions of a predetermined one of a security protocol. It only performs "per-flow ordering." See e.g., WO 0105086, page 9, lines 12-14, and page 3, lines 17-25.

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None of the elements, alone or in combination, of independent claim 7 of the Application are disclosed in WO 0105086. The rejection of claim 7 is unsupported by the cited art and should be withdrawn. As WO 0105086 does not anticipate independent claim 7, WO 0105086 cannot anticipate dependent claims 8-11. The rejection of claims 8-11 is unsupported by the cited art and should be withdrawn.

<u>Claims 12-14</u>

The same lines of text are cited as anticipating the "shared memory" element of independent claim 12 as were cited as anticipating the "memory" element of claim 1. As discussed above with respect to claim 1, the "memory" referred to at page 7, lines 23-26 is a "local memory" 160 associated with the cryptography acceleration chip 152 configuration of Fig. 1B. WO 0105086, page 7, lines 23-24. Referring to Fig. 1B, it is clear that memory 160 is merely communicatively coupled to the cryptography acceleration chip 152 *only*. There is no indication of memory 160 being "shared".

The passage at page 8, lines 22-29 refers to a memory used by a classification engine for performing "lookups from databases" stored there. Id., page 8, lines 21-22. This memory is communicatively coupled to either a memory controller 212 or directly to the cryptography engines 216 [sic] and packet classifier 204. Id. at lines 22-26. There is no discussion or diagram indicating that this memory is coupled to first and second processor cores as described in claim 12.

The text cited at page 2, lines 3-11 of WO 0105086 in no way describes "a multi-layer security services protocol partitioned between each of the first and second processor cores." No partitioning is described whatsoever. The text states, "[b]y incorporating both encryption and authentication functionality in a *single* accelerator chip, over-all system performance can be enhanced." WO 0105086, page 2, lines 5-6 (emphasis added).

The text at page 6, lines 19-20 cited by the Examiner states, "[t]he chip 102 on the card 103 may be connected to a system bus 104 via a standard system interface 106." (See Fig. 1A). This does not anticipate "one or more application program interfaces *operated by the first processor core for interfacing between the security services protocol and the second processor core*" as recited in claim 12. There is no "multi-layer security services protocol *partitioned between*" first and second processor cores in WO 0105086 at all. See also the discussion, *supra*, regarding claims 1 and 7.

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As discussed above with respect to claims 1 and 7, WO 0105086 only partitions processing in a horizontal fashion, i.e., "per-flow ordering." See e.g., WO 0105086, page 9, lines 12-14, and page 3, lines 17-25. There is no *multi-layer* security services protocol *partitioned* between processor cores.

The elements of independent claim 12 of the Application are not disclosed in WO 0105086. The rejection of claim 12 is unsupported by the cited art and should be withdrawn. As WO 0105086 does not anticipate independent claim 12, WO 0105086 cannot anticipate dependent claims 13-14. The rejection of claims 13-14 is unsupported by the cited art and should be withdrawn.

<div align="center">Claims 15-20</div>

As discussed above regarding claims 1-5 and 7-14, the cited art similarly does not anticipate Applicant's claims 15-20. Regarding independent claim 15, WO 0105086 does not describe a method that includes "partitioning a function of a multi-layer protocol in a first processor." The Office Action cites page 2, lines 3-11 and page 6, lines 22-26 as describing a method that anticipates this element. As discussed above, no partitioning of a multi-layer protocol is described whatsoever in WO 0105086. The text states, "[b]y incorporating both encryption and authentication functionality in a *single* accelerator chip, over-all system performance can be enhanced." WO 0105086, page 2, lines 5-6 (emphasis added). Regarding page 6, lines 22-26, neither of the named processors, 114 nor 108, are described as partitioning a function of a multi-layer protocol. Again, see the discussion, *supra*, regarding claims 1, 7, and 12.

The elements of independent claim 15 of the Application are not disclosed in WO 0105086. The rejection of claim 15 is unsupported by the cited art and should be withdrawn. As WO 0105086 does not anticipate independent claim 15, WO 0105086 cannot anticipate dependent claims 16-20. The rejection of claims 16-20 is unsupported by the cited art and should be withdrawn.

<div align="center">**Rejection Under 35 U.S.C. §103**</div>

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as unpatentable over WO 0105086. The Examiner took official notice that modular exponentiation used for encryption is well known in the cryptography art. The rejection is respectfully traversed. Applicant submits

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that the differences between the subject matter sought to be patented, and the reference cited by the Examiner, are not such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

As succinctly stated in the MPEP, to establish a *prima facie* case of obviousness, three basic criteria must be satisfied: (1) a suggestion or motivation to modify the cited reference; (2) a reasonable expectation of success; and (3) the cited reference must teach or suggest all the claim limitations. See MPEP §706.02(j). The cited reference "must expressly or impliedly suggest the claimed invention...."

Claim 6 depends on claim 5, which depends on claim 4, which depends on independent claim 1. All claim limitations of the rejected claim 6 must be considered, especially when one or more are missing from the cited prior art.

Applicants arguments, *supra*, regarding claim 1 clearly show that WO 0105086 does not anticipate claim 1. Thus, the cited art cannot anticipate the additional claim limitations of claim 4: "wherein the high performance processor further comprises a digital processor;" claim 5: "wherein the digital signal processor is further configured to operate a modular math function;" or claim 6: "wherein the digital signal processor is further configured to operate a modular math function comprising an exponentiation function," regardless of whether the Examiner takes official notice that modular exponentiation used for encryption is well known in the cryptography art. The obviousness rejection of claim 6 by the Examiner is unsupported by the cited art and should be withdrawn.

Conclusions

For the reasons set forth above, Applicant respectfully requests reconsideration and withdrawal of the foregoing rejections.

Applicant respectfully submits that the actions taken by Applicant do not raise new issues that would require further consideration or a new search and do not raise new matter.

In conclusion, Applicant asserts that this Response is complete as contemplated in 37 CFR §1.111, that claims 1-20 are patentable for the reasons set forth above, and that the Application is now in condition for allowance. Accordingly, Applicant respectfully requests an early notice of allowance.
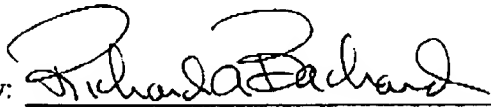
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Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

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